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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,274	12/17/2001	Wei-Kang King	17815-302101	4930

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/024,274	KING, WEI-KANG	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/568,933.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/17/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of the Group II invention, claim(s) 11-17 in the response filed on December 17, 2004, is acknowledged. The traversal is on the ground(s) that "it should be no undue burden on the Examiner to consider all claims in the single application." This is not found persuasive.

A restriction requirement between one set of product claims and a set of process claims was issued in the Office action mailed on November 17, 2004. "Section 121 [of Title 35 USC] permits a restriction for 'independent and distinct inventions,' which the PTO construes to mean that the sets of claims must be drawn to separately patentable inventions." See *Applied Materials Inc. v. Advanced Semiconductor Materials* 40 USPQ2d 1481, 1492 (Fed. Cir 1996)(Archer, C.J., concurring in-part and dissenting in-part). A product and the process of making the product are "two independent, albeit related inventions." See *In re Taylor*, 149 USPQ 615, 617 (CCPA 1966). "When two sets of claims filed in the same application are patentably distinct or represent independent inventions, the examiner is to issue a restriction requirement." See *In re Berg*, 46 USPQ2d 1226, 1233 n.10 (Fed. Cir. 1998).

The examiner, in issuing a restriction requirement, must demonstrate "one way distinctiveness." *Applied Materials Inc.* at 1492. As stated within the restriction requirement, "inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f))." In this application, the examiner restricted the product claims from

the process claims on the grounds that "the product as claimed can be made by another and materially different process such as a process wherein the device of Group I can be manufactured by selectively depositing a pad oxide layer pattern instead of forming a first pad oxide layer and a first mask layer and forming an opening in the first mask layer and removing the first pad oxide layer exposed by the opening to form cavity," and that, as a result, a restriction was necessary.

In addition to one way distinctiveness, the examiner must show "why it would be a burden to examine both sets of claims." *Applied Materials Inc.* at 1492. "A serious burden on the examiner may be *prima facie* shown if the examiner shows by appropriate explanation either separate classification, separate status in the art, or a different field of search." MPEP 803. An explanation was provided in the restriction requirement. Specifically, in addition to being distinct, the examiner indicated that restriction is proper because the product claims and the process claims "have acquired a separate status in the art."

The criteria of distinctness and burdensomeness have been met, as demonstrated hereinabove. Accordingly, the restriction requirement in this application is still deemed proper and is therefore **made FINAL.**

2. Claims 1-10 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention, the requirement having been traversed in the response filed on December 17, 2004.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11-13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US/5,913,133) in view of Wolf. (Silicon Processing for the VLSI Era Volume 3 – The Submicron MOSFET, Pages 362-365).

Re claim 11, Lee discloses a method for fabricating a field oxide on semiconductor substrate, comprising the steps of: forming successively a first pad layer (22) and a first mask layer (23); forming an opening (not labeled) in the first mask layer (23) to define a region for forming the field oxide (not labeled); removing the first pad layer (22) exposed by the opening to form a cavity (not labeled); forming a mask (25) portion in the sidewall of the patterned first mask (23) layer and the cavity (22); and carrying out thermal oxidation to form the field oxide (26) in the opening (see Lee Figs. 2A – 2F).

However, Lee does not specifically disclose forming a second pad layer having a smaller thickness than the first pad layer on the semiconductor substrate and isotroically etching the second layer to leave a mask filler in the cavity.

Wolf discloses processing method including forming of substrate, first pad layer, mask layer and forming of a second pad layer having a smaller thickness than the first pad layer on the semiconductor substrate (see Figs. 6-34 through 6-38 and Pages 362-365). Wolf discloses " the exposed portions of Si including the undercut portions were oxidized to grow a very thin oxide as a new buffer layer." In addition Wolf disclosed isotropically etching the second mask layer to leave a mask filler in the cavity (See Wolf Page 363, and see Fig 6-38).

Both Lee and Wolf teachings are directed to local oxidation process for the fabrication of MOSFET. Therefore, the teachings of Lee and Wolf are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Lee reference with second pad layer (i.e. thermally grown oxide layer) as taught by Wolf in order to use the second pad layer that remain in the grove as a buffer layer during thermal oxidation process to form FOX region (see Wolf Page 363, and see Fig 6-38).

Re claim 12, as applied to claim 11 above Lee and Wolf in combination teach all the claimed limitations including the limitation removing the first pad layer exposed by the opening to form a cavity labeled by wet etching (see Lee Figs. 2B, 2C and Col. 3, lines 1-4 and Wolf Fig. 6-38).

Re claim 13, as applied to claim 11 above Lee and Wolf in combination teach all the claimed limitations including the limitation forming a second pad layer having a smaller thickness than the first pad layer on the semiconductor substrate by thermal oxidation (see Lee Fig 2F and Col. 3, lines 25-27 and Wolf Fig. 6-38).

Re claim 17, Lee discloses a method for fabricating a field oxide on semiconductor substrate, comprising the steps of: forming successively a first pad layer (22) and a first mask layer (23); forming an opening (not labeled) in the first mask layer (23) to define a region for forming the field oxide (not labeled); removing the first pad layer (22) exposed by the opening to form a cavity (not labeled); forming a mask (25) portion in the sidewall of the patterned first mask (23) layer and the cavity (22); and carrying out thermal oxidation to form the field oxide (26) in the opening (see Lee Figs. 2A – 2F).

However, Lee does not specifically disclose forming a second pad layer having a smaller thickness than the first pad layer on the semiconductor substrate and isotroically etching the second layer to leave a mask liner on the sidewall having a width 0 to 50 angstroms and a mask filler in the cavity.

Wolf discloses processing method including forming of substrate, first pad layer, mask layer and forming of a second pad layer having a smaller thickness than the first pad layer on the semiconductor substrate (see Figs. 6-34 through 6-38 and Pages 362-365). Wolf discloses " the exposed portions of Si including the undercut portions were oxidized to grow a very thin oxide as a new buffer layer." In addition Wolf disclosed isotropically etching the second mask layer to form a liner having a predetermined thickness and a mask filler in the cavity (See Wolf Page 363, and see Fig 6-38).

Both Lee and Wolf teachings are directed to local oxidation process for the fabrication of MOSFET. Therefore, the teachings of Lee and Wolf are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Lee reference with second pad layer (i.e. thermally grown oxide layer) as taught by Wolf in order to use the second pad layer that remain in the grove as a buffer layer during thermal oxidation process to form FOX region (see Wolf Page 363, and see Fig 6-38).

Furthermore, the claimed thickness rage would have been achieved by one having ordinary skill in the art by routine optimization by controlling the etch rate.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not

disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

5. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US/5,913,133) and Wolf. (Silicon Processing for the VLSI Era Volume 3 – The Submicron MOSFET, Pages 362-365), as applied to claims 11-13 in Paragraph 4 above, and further in view of Chien et al. (US/5,643,824).

Re claims 14 –16, as applied to claim 11 in Paragraph 4 above, Lee and Wolf in combination teach all the claimed limitations including using of reactive ion etching (RIE) process using the known plasma etchant.

However, the combination do not specifically disclose the use of the fluorine-containing gas such as NF_3, SF_6 and CF_4.

Chien et al. disclose utilizing of fluorine-containing etching such as NF_3, SF_6 and CF_4 because of its silicon selectivity to oxide or nitride (see Chien et al. Col. 5, line 65 – Col. 6, line 11).

Lee, Wolf and Chien et al. teachings are directed to local oxidation process for the fabrication of MOSFET. Therefore, the teachings of Lee, Wolf and Chien et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Lee and Wolf reference with use of the fluorine-containing gas such as NF_3, SF_6 and CF_4 as taught by Chien et al. because of the etchants etch selectivity toward silicon comparing to oxide or nitride.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Gray et al. (US/5,534,107) also disclose similar inventive subject matter.

Correspondence

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823

Brook Kebede

BK
February 22, 2005